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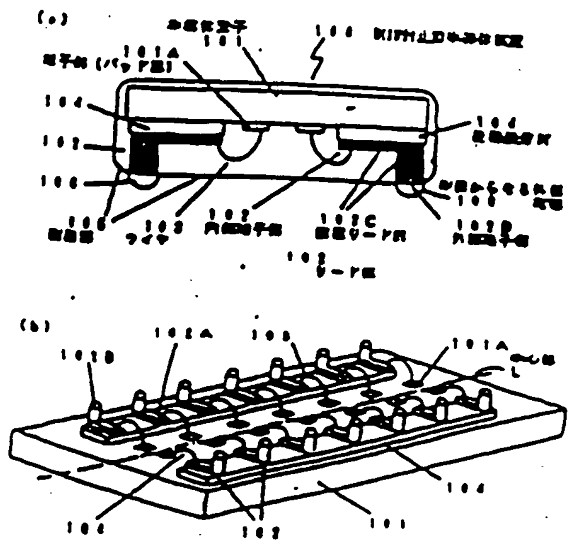
(54)【発明の名称】樹脂封止型半導体装置とそれに用いられるリードフレーム、及び樹脂封止型半導体装置の製造方法

(57)【要約】

【目的】　更なる樹脂封止型半導体装置の高集積化、高機能化が求められている中、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応させ、同時に従来のTSOP等の小型パッケージに困難であった更なる多ピン化を実現した樹脂封止型半導体装置を提供する。

【構成】　半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する連結リード部とを一体とした複数のリード部とを、絶縁性接着材層を介して、固着して設けており、且つ、回路基板等への実装のための半田からなる外部電極を前記複数の各リードの外部端子部に連結させ、少なくとも前記半田からなる外部電極の一部に樹脂部より外部に露出させて設けている。



【特許請求の範囲】

【請求項1】　半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体としたリード部を複数個、絶縁性接着材層を介して、固着して設けており、且つ、回路基板等への実装のための半田からなる外部電極を前記複数のリードの外部端子部に連結させ、少なくとも前記半田からなる外部電極の一部は樹脂部より外部に露出させて設けていることを特徴とする樹脂封止型半導体装置。

【請求項2】　請求項1において、半導体素子の端子は半導体素子の端子面の一対の辺の略中心線上にそって配置されており、リード部は複数の端子を挟むように対向し前記一対の辺に沿い設けられていることを特徴とする樹脂封止型半導体装置。

【請求項3】　半導体素子の端子と電気的に接続するための内部端子部と、外部回路と接続するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から直交する一方の側に突出させ、対向し先端部同士で連結部を介して連結する一対の内部端子部を複数設けており、且つ、各外部端子部の外側で、接続リード部と連結し、一体として全体を保持する外枠部を設けていることを特徴とするリードフレーム。

【請求項4】　半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした複数のリード部とを、絶縁性接着材層を介して、固着して設けており、且つ、回路基板等への実装のための半田からなる外部電極を前記複数のリードの外部端子部に連結させ、少なくとも前記半田からなる外部電極の一部は樹脂部より外部に露出させて設けている樹脂封止型半導体装置の製造方法であって、少なくとも、（A）エッチング加工にて、半導体素子の端子と電気的に接続するための内部端子部と、外部回路と接続するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から直交する一方の側に突出させ、対向し先端部同士で連結部を介して連結する一対の内部端子部を複数設けており、且つ、各外部端子部の外側で、接続リード部と連結し、一体として全体を保持する外枠部を設けているリードフレームを作製する工程、（B）リードフレームの外部端子突出側でない面（裏面）に接着材を設け、打ち抜き金型により、対向する内部端子同士を連結する連結部と該連結部に対応する位置に設けられた接着材とを打ち抜き、リードフレームの打ち抜かれた部分が半導体素子の端子部にくるようにして、接着材を介して、リードフレーム全体を半導体素子へ固着する工程、（C）リードフレームの外枠部を含む不要の部分を打ち抜き金型により切断除去する工程、（D）半導体素子の端子部と、切断されて、半導体素子へ固着された内部端子部の先端部とをワイヤボンディングした後に、樹脂により外部端子部の先を外部に露出させて全体を封止する工程、（E）前記外部に露出した外部端子部面に半田からなる外部電極を作製する工程、とを含むことを特徴とする樹脂封止型半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体素子を搭載する樹脂封止型の半導体装置（プラスチックパッケージ）に関し、特に、実装密度を向上させ、且つ、多ピン化に対応できる半導体装置とその製造方法に関する。

【0002】

【従来の技術】近年、半導体装置は、高集積化、小型化技術の進歩と電子機器の高性能化と軽薄短小化の傾向（時流）から、ＬＳＩのＡＳＩＣに代表されるように、ますます高集積化、高機能化になってきている。これに伴い、リードフレームを用いた封止型の半導体装置プラスチックパッケージにおいても、その開発のトレンドが、ＳＯＪ（Ｓｍａｌｌ　Ｏｕｔｌｉｎｅ Ｊ－Ｌｅａｄｅｄ　Ｐａｃｋａｇｅ）やＱＦＰ（Ｑｕａｄ　Ｆｌａｔ　Ｐａｃｋａｇｅ）のような表面実装型のパッケージを経て、ＴＳＯＰ（Ｔｈｉｎ　Ｓｍａｌｌ　Ｏｕｔｌｉｎｅ　Ｐａｃｋａｇｅ）の開発による薄型化を主体としたパッケージの小型化へ、さらにはパッケージ内部の３次元化によるチップ収納効率向上を目的としたＬＯＣ（Ｌｅａｄ　Ｏｎ　Ｃｈｉｐ）の構造へと進展してきた。しかし、樹脂封止型半導体装置パッケージには、高集積化、高機能化とともに、更に一層の多ピン化、薄型化、小型化が求められており、上記構造のパッケージにおいてもチップ外周部分のリードの引き回しがあるため、パッケージの小型化に限界が見えてきた。また、ＴＳＯＰ等の小型パッケージにおいては、リードの引き回し、ピンピッチから多ピン化に対しても限界が見えてきた。

【0003】

【発明が解決しようとする課題】上記のように、更なる樹脂封止型半導体装置の高集積化、高機能化が求められており、樹脂封止型半導体装置パッケージの一層の多ピン化、薄型化、小型化が求められている。本発明は、このような状況のもと、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応させ、回路基板への実装面積を低減できる、即ち、回路基板への実装密度を向上させることができる樹脂封止型半導体装置を提供しようとするものである。また、同時

に従来のTSOP等の小型パッケージに匹敵でもった更なる多ピン化を実現しようとするものである。

【0004】

【課題を解決するための手段】本発明の樹脂封止型半導体装置は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした複数のリード部とを、絶縁性接着材層を介して、固着して設けており、且つ、回路基板等への実装のための半田からなる外部電極を前記複数の各リードの外部端子部に連結させ、少なくとも前記半田からなる外部電極の一部は樹脂部より外部に露出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした複数のリード部の配列を半導体素子の端子側面上に二次元的に配列し、外部電極部を半田ボールにて形成することによりBGA(Ball Grid Array)タイプの樹脂封止型半導体装置とすることもできる。

【0005】そして、上記において、半導体素子の端子は半導体素子の端子面の一対の辺の略中心線上にそって配置されており、リード部は複数の端子を挟むように対向し前記一対の辺に沿い設けられていることを特徴とするものである。また、本発明のリードフレームは、樹脂封止型半導体装置用のリードフレームであって、半導体素子の端子と電気的に接続するための内部端子部と、外部回路と接続するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から直交する一方向側に突出させ、対向し先端部同士で連結部を介して接続する一対の内部端子部を複数設けており、且つ、各外部端子部の外側で、接続リード部と連結し、一体として全体を保持する外枠部を設けていることを特徴とするものである。尚、上記リードフレームにおいて、内部端子部と外部端子部とそれを連結する接続リード部とを一体とした組みを複数リードフレーム面に二次元的に配列するして形成することによりBGA(Ball Grid Array)タイプの樹脂封止型半導体装置用のリードフレームとすることもできる。

【0006】本発明の樹脂封止型半導体装置の製造方法は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした複数のリード部とを、絶縁性接着材層を介して、固定して設けており、且つ、回路基板等への実装のための半田からなる外部電極を前記複数の各リードの外部端子部に連結させ、少なくとも前記半田からなる外部電極の一部は樹脂部より外部に露出させて設けている樹脂封止型半導体装置の製造方法であって、少なくとも、(A)エッチング加工にて、半導体素子の端子と電気的に接続するための内部端子部と、外部回路と接続するための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から直交する一方向側に突出させ、対向し先端部同士で連結部を介して接続する一対の内部端子部を複数設けており、且つ、各外部端子部の外側で、接続リード部と連結し、一体として全体を保持する外枠部を設けているリードフレームを作製する工程、(B)前記リードフレームの外部端子部側でない面(裏面)に絶縁材を設け、打ち抜き金型により、対向する内部端子部同士を連結する連結部と該連結部に対応する位置に設けられた絶縁材とを打ち抜き、リードフレームの打ち抜かれた部分が半導体素子の端子部にくるようにして、前記絶縁材を介して、リードフレーム全体を半導体素子へ固着する工程、(C)リードフレームの外枠部を含む不要の部分を打ち抜き金型により切断除去する工程、(D)半導体素子の端子部と、切断されて、半導体素子へ固着された内部端子部の先端部とをワイヤボンディングした後に、樹脂により外部端子部面のみを外部に露出させて全体を封止する工程、(E)前記外部に露出した外部端子部面に半田からなる外部電極を作製する工程、とを含むことを特徴とするものである。

【0007】

【作用】本発明の樹脂封止型半導体装置は、上記のような構成にすることにより、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応できるものとしている。即ち、半導体装置の回路基板への実装面積を縮小し、回路基板への実装密度の向上を可能としている。詳しくは、内部端子部、外部端子部とを一体とした複数のリード部を半導体素子面に絶縁接着材層を介して固定し、前記外部端子部に半田からなる外部電極部を連結させていることより、装置の小型化を達成している。そして、上記半田からなる外部電極部を、半導体素子面に略平行な面で二次元的に配列することにより、半導体装置の多ピン化を可能としている。半田からなる外部電極部を半田ボールとし、二次元的に該外部電極部を配列した場合にはBGAタイプとなり、半導体装置の多ピン化にも対応できる。また、上記において、半導体素子の端子が半導体素子の端子面の一対の辺の略中心線上にそって配置され、リード部は複数の端子を挟むように対向し前記一対の辺に沿い設けられており、簡単な構造とし、量産性に適した構造としている。本発明のリードフレームは、上記のような構成にすることにより、上記樹脂封止型半導体装置の製造を可能とするものであるが、通常のリードフレームと同様のエッチ

とができる。本発明の樹脂封止型半導体装置の製造方法は、上記リードフレームを用いて、リードフレームの外部端子形成でない面（裏面）に絶縁材を右に、打ち抜き金型により、対向する内部端子部同士を接続する連結部と該連結部に対応する位置に設けられた絶縁材とを打ち抜き、リードフレームの打ち抜かれた部分が半導体素子の端子部にくるようにして、前記接着材を介して、リードフレーム全体を半導体素子へ搭載し、リードフレームの外枠部を含む不要の部分を打ち抜き金型により切断除去することにより、内部端子と外部端子を一体とした組みを多数半導体素子上に搭載した、本発明の、半導体装置の小型化が可能な、且つ、多ピン化が可能な樹脂封止型半導体装置の作製を可能としている。

【0008】

【実施例】本発明の樹脂封止型半導体装置の実施例を以下、図にそって説明する。図1（a）は本実施例樹脂封止型半導体装置の断面概略図であり、図1（b）は要部の平面図である。図1中、100は樹脂封止型半導体装置、101は半導体素子、102はリード部、102Aは内部端子部、102Bは外部端子部、102Cは段差リード部、101Aは端子部（パッド部）、103はワイヤ、104は絶縁接着材、105は樹脂部、106は半田（ペースト）からなる外部電極である。本実施例樹脂封止型半導体装置は、後述するリードフレームを用いたもので、内部端子部102A、外部端子部102Bを一体としたL字型のリード部102を多数半導体素子101上に絶縁接着材104を介して搭載し、且つ、外部端子部102B先に半田からなる外部電極を樹脂部105より外部へ突出させて設けた、パッケージ面積が略半導体素子の面積に相当する樹脂封止型半導体装置であり、回路基板へ搭載される際には、半田（ペースト）を溶融、固化して、外部端子部102Bが外部回路と電気的に接続される。本実施例樹脂封止型半導体装置は、図1（b）に示すように、半導体素子101の端子部（パッド部）101Aは半導体素子の中心線Lをはさみ対向して2個づつ、中心線Lに沿って配置されており、リード部102も、内部端子部102Aが前記端子部（パッド部）に沿った位置に半導体素子101の面の外側に中心線を挟み対向するように配置されている。外部端子部102Bは内部端子部102Aから段差リード部102Cを介して離れて位置し、ほぼ半導体素子の側面までに至った位置で半導体素子平面に垂直する方向に、段差リード102CがL字に曲がり、外部端子部102Bはその先端に位置し、半導体素子の面に平行な面方向で一次元的に配列をしている。即ち、中心線Lを挟み2列の外部端子部102Bの配列を設けている。そして、各外部端子に連結させ、半田（ペースト）からなる外部電極106を樹脂部105より外部に露出させて設けている。尚、絶縁接着材104としては、100μm厚のポリイミド系の熱可塑性接着剤HM122C（日立化成工業株式会社）を用いたが、他には、シリコン変性ポリイミドTA1715（住友ベークライト株式会社）や熱硬化型接着剤HCS200（信越化学工業株式会社）等が挙げられる。上記実施例では、半田ペーストからなる外部電極であるが、この部分は半田ボールに代えても良い。尚、本実施例樹脂封止型半導体装置は、上記のように、パッケージ面積が略半導体装置の面積に相当する、極端に小型化されたパッケージであるが、厚み方向についても、約1．0mm厚以下にすることができ、薄型化も同時に達成できるものである。本実施例においては外部電極部を、半導体素子の端子部（パッド部）に沿い2列に配列したが、半導体素子の端子の位置を二次元的に配置し、内部端子部と外部端子部との一体となった組みを複数、半導体素子の端子面側に二次元的に配列して搭載することにより、半導体素子の、一層の多ピン化に十分対応できる。

【0009】次いで、本発明のリードフレームの実施例を挙げ、図にもとづいて説明する。本実施例リードフレームは、上記実施例半導体装置に用いられたものである。図2に実施例リードフレームの平面図を示すもので、図2中、200はリードフレーム、201は内部端子部、202は外部端子部、203は段差リード部、204は連結部、205は外枠部である。リードフレームは42合金（Ni42%のFe合金）からなり、リードフレームの厚さは、内部端子部のある周辺部で0．05mm、外部端子部のある周辺部で0．2mmである。内部端子部の対向する先端部同士を連結する連結部205も同厚（0．05mm厚）に形成されており、後述する半導体装置を作製する際の打ち抜き金型にて打ち抜きし易い構造となっている。本実施例では外部端子部202は丸状であるが、これに限定はされない。また、リードフレーム素材として42合金を用いたがこれに限定されない。銅系合金でも良い。

【0010】次に、上記実施例リードフレームの製造方法を図を用いて簡単に説明する。図4は本実施例リードフレームを製造した工程を示したものである。先ず、42合金（Ni42%のFe合金）からなる、厚さ0．2mmのリードフレーム素材300を準備し、板の両面を脱脂等を行い良く洗浄処理した（図3（a））後、リードフレーム素材300の両面に感光性のレジスト301を塗布し、乾燥した。（図3（b））。
次いで、リードフレーム素材300の両面から所定のパターン版を用いてレジストの所定の部分のみに露光を行った後、現像処理し、レジストパターン301Aを形成した。（図3（c））
尚レジストとしては東京応化工業株式会社のネガ型感光性レジスト（PMERレジスト）を使用した。次いで、レジストパターン301Aを耐腐蝕膜として、57°C、48ボーメの塩化第二鉄水溶液にて、リードフレーム素材300の両面からスプレイエッチングして、内部端

の平面図が図2に示されたリードフレームを作製した（図3（c））。図2（b）のは、図2のA1－A2における断面図である。この後、レジストを除去した後、洗浄処理を施した後、所定の箇所（内部端子部分を含む領域）のみに金メッキ処理を行った。（図3（e））

尚、上記リードフレームの製造工程においては、図2（b）に示すように、薄肉部と厚肉部を形成するため、外部端子形成面側からのエッチング（腐蝕）を多く行い、反対面側からは少なめにエッチング（腐蝕）を行った。また、金メッキに代え、銀メッキやパラジウムメッキでも良い。上記のリードフレームの製造方法は、1ケの半導体装置を作製するために必要なリードフレーム1ケの製造方法であるが、通常は生産性の面から、リードフレーム素材をエッチング加工する際、図2に示すリードフレームを複数個面付けした状態で作製し、上記の工程を行う。この場合は、図2に示す外枠部205の一部に連結する枠部（図示していない）をリードフレームの外側に設けて面付け状態とする。

【0011】次に、上記のようにして作製されたリードフレームを用いた、本発明の樹脂封止型半導体装置の製造方法の実施例を図にそって説明する。図4は、本実施例樹脂封止型半導体装置の製造工程を示すものである。図3に示すようにして作製されたリードフレーム400の外部端子部402形成面（表面）と対向する裏面に、ポリイミド系熱硬化型の絶縁接着材（テープ）401（日立化成株式会社製、HM122C）を、400°C、6Kg/m'で1.0秒熱圧着して貼りつけた（図4（a））。この状態の平面図を図5に示す。この後打ち抜き金型405A、405Bにて（図4（b））、対向する内部端子部の先端部を連結する連結部403と、その部分の絶縁接着材（テープ）401とを打ち抜いた。（図4（c））

次いで、外枠打ち抜きおよび圧着用金型406A、406Bを用い、外枠部404を含む不要の部分を切り離す（図4（d））と同時に、絶縁接着材404を介して半導体素子407上にリード部408の熱圧着を行った。（図4（e））

尚、この図4（d）に示す、内部リードと連結してリードフレーム全体を支えている外枠部204を含む不要の部分を切り離しは、樹脂封止した後に行っても良い。この場合には、通常の単層リードフレームを用いたQFPパッケージ等のようにダムバー（図示していない）を設けると良い。リード部410を半導体素子411へ圧着した後、ワイヤー414により、半導体素子の端子（パッド）411Aとリード部410の内部端子410Aとを電気的に結線した。（図4（f））

その後、所定の金型を用い、エポキシ系の樹脂415でリード部410の外部端子部410Bのみを露出させて、全体を封止した。（図4（g））

ここでは、専用の金型（図示していない）を用いたが、所定の面（外部端子面）を残し樹脂封止できれば、とくに金型は必要としない。次いで、露出されている外部端子部410B上に半田ペーストをスクリーン印刷により塗布し、半田（ペースト）からなる外部電極416を作製し、本発明の樹脂封止型半導体装置を作製した。（図4（h））

尚、半田からなる外部電極416の作製は、スクリーン印刷に限定されるものではなく、リフロー又はポッティング等でも、回路基板と半導体装置との接続に必要な量の半田が得られれば良い。

【0012】

【発明の効果】本発明は、上記のように、更なる樹脂封止型半導体装置の高集積化、高機能化が求められる状況のもと、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応させ、回路基板への実装面積を縮減できる。即ち、回路基板への実装密度を向上させることができる半導体装置の提供を可能としたものであり、同時に従来のTSOP等の小型パッケージに困難であった更なる多ピン化を実現した樹脂封止型半導体装置の提供を可能としたものである。

【図面の簡単な説明】

【図1】実施例の樹脂封止型半導体装置の概略断面図及び要部拡大図

【図2】実施例のリードフレームの平面図

【図3】実施例のリードフレームの製造工程図

【図4】実施例の樹脂封止型半導体装置の製造工程図

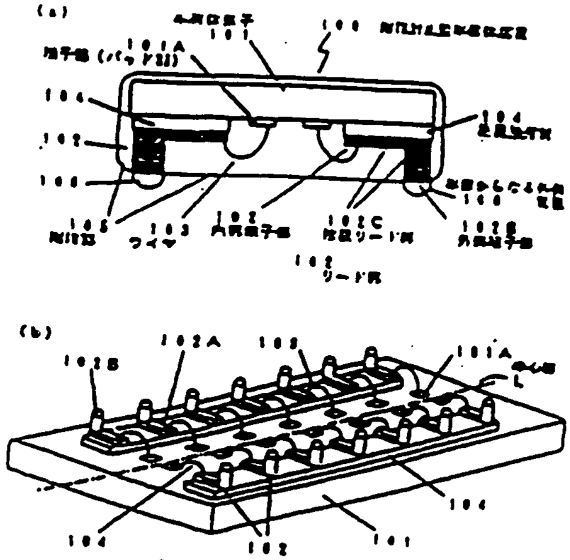
【図5】実施例のリードフレームに絶縁接着材を貼りつけた状態の平面図

【符号の説明】

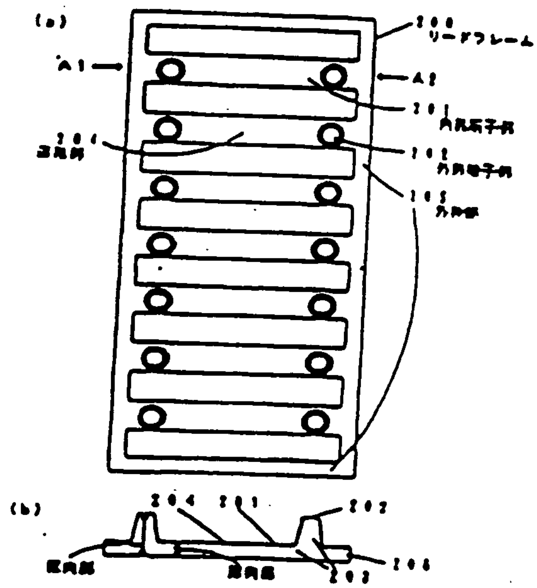
100	樹脂封止型半導体装置
101	半導体素子
101A	端子部（パッド部）
102	リード部
102A	内部端子部
102B	外部端子部
102C	[illegible]リード部
103	ワイヤ
104	絶縁接着材
105	樹脂部
106	半田（ペースト）からなる外部電極
200	リードフレーム
201	内部端子部
202	外部端子部
203	[illegible]リード部
204	連結部
205	外枠部
300	リードフレーム素材
301	レジスト
[illegible]	[illegible]

303A	内部端子部
303B	外部端子部
304	屈曲部
305	金メッキ部
306	外枠部
400	リードフレーム
401	絶縁性部材（テープ）
402	外部端子部
403	屈曲部
405A、405B	打ち抜き穴
406A、406B	外枠打ち抜きおよび圧着用穴
410	リード部
410A	内部端子部
410B	外部端子部
410C	接続リード部
411	半導体素子
411A	ワイヤー
415	樹脂

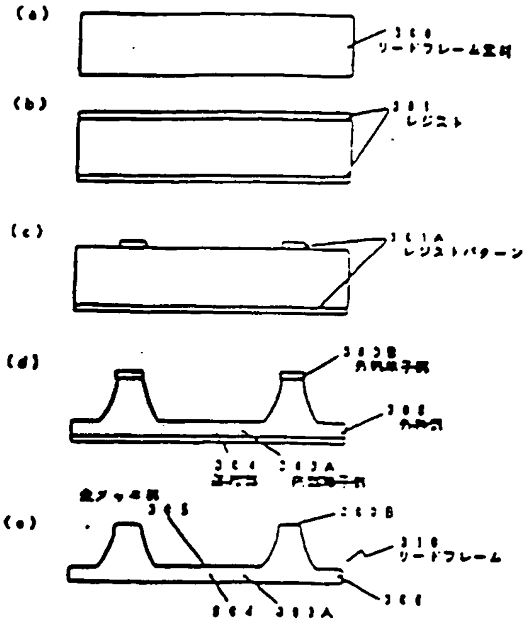
【図1】



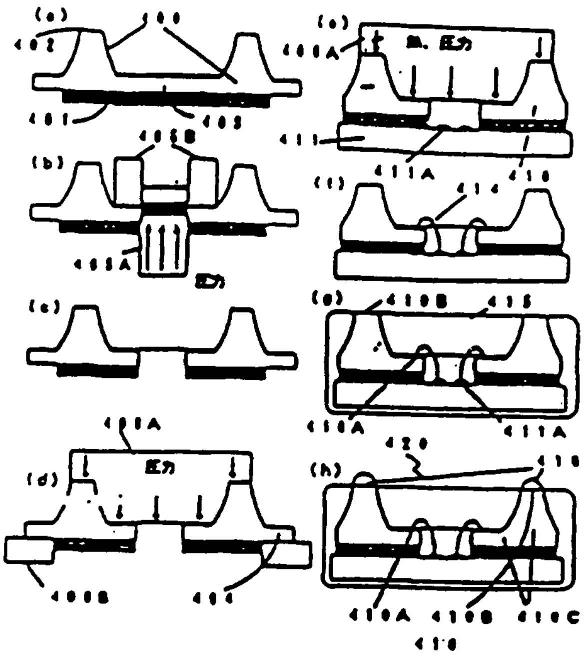
【図2】



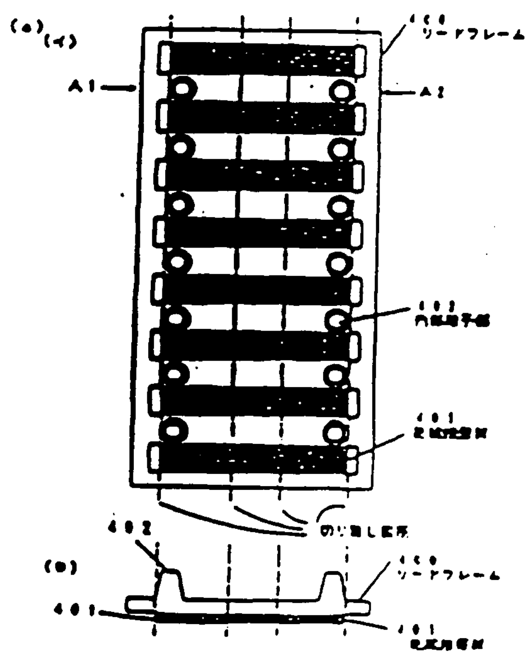
〔図3〕


(a)
300 リードフレーム素材
(b)
301 レジスト
(c)
301A レジストパターン
(d)
303B 内部端子部
(e)
310 リードフレーム

〔図4〕


(a)
(b)
圧力
(c)
(d)
圧力
(e)
熱、圧力
(f)
(g)
(h)
410A
410B
410C

〔図5〕


(a)
(イ)
A1
A2
400 リードフレーム
402 内部端子部
(ロ)
402
400 リードフレーム
401

Japanese Patent Laid-Open Publication No. Heisei 8-125066

[TITLE OF THE INVENTION]

Resin Encapsulated Semiconductor Device, Lead Frame Used Therein, and Fabrication Method for the Resin Encapsulated Semiconductor Device

[CLAIMS]

1. A resin encapsulated semiconductor device comprising:

a semiconductor chip;

a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and

outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of

solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate.

2. The resin encapsulated semiconductor device according to claim 1, wherein the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets.

3. A lead frame comprising:

a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other;

each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame

surface via an associated one of the connecting lead portions;

the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively;

connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and

an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame.

4. A method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit,

and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of:

(A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions,- the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form

an integral structure together, thereby protecting the entire portion of the lead frame;

(B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween;

(C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions;

(D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and encapsulating the semiconductor chip and the lead frame by a resin while allowing a surface of the lead frame toward the outer terminal portions to be externally exposed; and

(E) forming outer electrodes made of solder on the exposed lead frame surface toward the outer terminal portions.

(DETAILED DESCRIPTION OF THE INVENTION)

(FIELD OF THE INVENTION)

The present invention relates to a resin encapsulated semiconductor device (plastic package) in which a semiconductor chip is packaged, and more particularly to a semiconductor device configured to achieve an improvement in mounting density or to have a multi-pinned structure and a method for manufacturing such a semiconductor device.

(DESCRIPTION OF THE PRIOR ART)

Recently, semiconductor devices have been developed to have a higher integration degree and a higher performance by virtue of developments of techniques associated with an increase in integration degree and miniaturization and in pace with the tendency of electronic appliances to have a high performance and a light, thin, simple, and miniature structure. A representative example of such semiconductor devices is an ASIC of LSI. For instance, developments of resin encapsulated semiconductor device plastic packages have been advanced from surface-mounting packages such as SOJs (Small Outlined-Leaded Packages) or QFPs (Quad Flat Packages) to packages having a miniature structure mainly achieved in accordance with a thinness obtained by virtue of developments of TSOPs (Tin Small Outline Packages) or to LOC (Lead On Chip) structures

adapted to achieve an improvement in the chip packaging efficiency by virtue of developments of an internal three-dimensional package structure. In addition to an increase in integration degree and improvement in performance, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In the above mentioned conventional packages, however, there is a limitation in miniaturization because those packages have a structure in which leads are arranged around a chip. Similarly, leads are arranged around a chip in the case of miniature packages such as TSOPs. In such packages, there is also a limitation in increasing the number of pins due to the pin pitch used.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

As mentioned above, there has been demand for an increase in integration degree and improvement in performance of resin encapsulated semiconductor devices. Also, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In such situations, the present invention makes it possible to increase the occupancy degree of a chip in a semiconductor package with a limited size while reducing the mounting area of the

semiconductor package on a circuit board to achieve a miniaturization of the resulting semiconductor device. That is, the present invention is adapted to provide a resin encapsulated semiconductor device capable of achieving an improvement in the mounting density thereof on a circuit board. Also, the present invention is adapted to achieve an increase in the number of pins which is difficult in miniature packages such as conventional TSOPs.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

The resin encapsulated semiconductor device of the present invention is characterized in that it comprises: a semiconductor chip; a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the

leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate. The above semiconductor device can be embodied into a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The above semiconductor device is also characterized in that the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. The lead frame of the present invention is characterized in that it comprises: a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be

connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions; the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively; connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame. The above lead frame can be embodied into a lead frame for a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The present invention is also characterized by a method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached

to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of: (A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a

lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame; (B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween; (C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions; (D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and

encapsulating the semiconductor chip and the lead frame by a resin while allowing a surface of the lead frame toward the outer terminal portions to be externally exposed; and (E) forming outer electrodes made of solder on the exposed lead frame surface toward the outer terminal portions.

[FUNCTIONS]

With the above mentioned configuration, the resin encapsulated semiconductor device of the present invention can increase the occupancy degree of the chip while achieving a miniaturization thereof. That is, the resin encapsulated semiconductor device is capable of reducing the mounting area thereof on a circuit board and achieving an improvement in the mounting density thereof on the circuit board. In particular, the present invention achieves a miniaturization of the semiconductor device by fixedly attaching a plurality of leads each including an inner terminal portion and an outer terminal portion integral with each other to a surface of a semiconductor chip by an insulating adhesive layer interposed between the semiconductor chip and the leads, and connecting outer electrodes made of solder to the outer terminal portions, respectively. Also, the present invention achieves an increase in the number of pins in the semiconductor device by arranging the outer electrodes made of solder in a two-

dimensional fashion on a plane parallel to the surface of the semiconductor chip. Where the outer electrodes made of solder are formed in the form of solder balls and arranged in a two-dimensional fashion, a BGA type semiconductor device capable of achieving an increase in the number of pins can be obtained. In the above semiconductor device, the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. Thus, the semiconductor device has a simple structure suitable in regard to productivity. The lead frame of the present invention makes it possible to fabricate the above mentioned resin encapsulated semiconductor device by virtue of there above mentioned configuration thereof. However, this lead frame can be fabricated using a half etching method during an etching process as used for conventional lead frames. The method for fabricating a resin encapsulated semiconductor device in accordance with the present invention involves the steps of applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out

the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween, and cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions. Thus, a plurality of leads each including an inner terminal portion and an outer terminal portion integral with each other are mounted on a semiconductor chip. Accordingly, the present invention makes it possible to achieve a miniaturization of semiconductor devices. In accordance with the present invention, it is also possible to fabricate a resin encapsulated semiconductor device having an increased number of pins.

[EMBODIMENTS]

Hereinafter, embodiments of the present invention associated with resin encapsulated semiconductor devices will be described in conjunction with the annexed drawings. Fig. 1A is a cross-sectional view schematically

illustrating a resin encapsulated semiconductor device according to an embodiment of the present invention. Fig. 1B is a perspective view illustrating an essential part of the resin encapsulated semiconductor device. Figs. 1A and 1B, the reference numeral 100 denotes the resin encapsulated semiconductor device, 101 a semiconductor chip, 102 leads, 102A inner terminal portions, 102B outer terminal portions, 102C connecting lead portions, 101A contacts (pads), 103 wires, 104 an insulating adhesive, 105 a resin encapsulate, 106 outer electrodes made of solder (paste), respectively. The resin encapsulated semiconductor device according to this embodiment is fabricated using a lead frame which will be described hereinafter. In this resin encapsulated semiconductor device, a plurality of L-shaped leads 102, each of which has an inner terminal portion 102A and an outer terminal portion 102 integral with each other, are mounted on a semiconductor chip 101 by means of an insulating adhesive 104. An outer electrode 106, which is made of solder, is attached to each outer terminal portion 102B. The outer electrode 106 is outwardly protruded from a resin encapsulate 105. The resin encapsulated semiconductor device configured as mentioned above has a package area substantially equal to the entire area thereof. When this semiconductor device is mounted on a circuit board, the

solder is melted and then solidified to allow the outer terminal portions 102B to be electrically connected to an external circuit. In the resin encapsulated semiconductor device according to the illustrated embodiment, contacts (pads) 101A provided at the semiconductor chip 101 are arranged in pairs along a center line L of the semiconductor chip 101 at opposite sides of the center line L in such a fashion that contacts included in each contact pair face each other. The outer terminal portion 102B of each lead is spaced apart from the inner terminal portion 102A of the lead. Between the inner and outer terminal portions 102A and 102B, a connecting lead portion 102C is interposed. The connecting lead portion 102C of each lead is bent in a direction orthogonal to the major surface of the semiconductor chip at a position near an associated one of the side surfaces of the semiconductor chip 101, so that it has an L shape. In each lead, the outer terminal portion 102B is arranged at an end of the connecting lead portion 102C. The outer terminal portions 102B of the leads are arranged in a one-dimensional fashion on a plane parallel to the major surface of the semiconductor chip 101. That is, the outer terminal portions 102B are arranged in two lines at opposite sides of the center line L. As mentioned above, one outer electrode 106 made of solder is connected to the outer terminal portion 102B of

each lead and outwardly exposed from the resin encapsulate 105.

For the insulating adhesive 104, a polyimide-based thermoplastic adhesive having a thickness of 100 μm (HM122C manufactured by Hitachi Chemical Co., Ltd.) is preferably used. Alternatively, a silicon denaturalized polyimide adhesive (ITA1715 manufactured by Sumitomo Bakelite Co., Ltd.) or a thermosetting adhesive (HG5200 manufactured by Tomoekawa Papermaking Co., Ltd.) may be used. Although outer electrodes made of solder paste are used in the illustrated embodiment, solder balls may be used.

As mentioned above, the resin encapsulated semiconductor device according to the illustrated embodiment has a package area substantially equal to the entire area thereof. That is, the illustrated embodiment of the present invention provides a package having a compact structure in regard to area. In accordance with the present invention, a thinned package structure can also be provided in that it is also possible to reduce the package thickness to about 1.0 mm or less. Although the outer electrodes have been described as being arranged in two lines along the contacts (pads) of the semiconductor chip, they may be arranged in a two-dimensional fashion. This is achieved by arranging contacts of the semiconductor chip in a two-dimensional fashion. On the surface of the

semiconductor chip arranged with those contacts, a plurality of terminal sets each having an inner terminal and outer terminal integral with each other are arranged in a two-dimensional fashion. In this case, it is possible to fabricate a semiconductor device using a semiconductor chip with an increased number of pins.

An embodiment of the present invention associated with a lead frame will now be described. The lead frame according to this embodiment is adapted to be used in the above mentioned semiconductor device. Fig. 2 is a plan view of the lead frame according to this embodiment. In Fig. 2, the reference numeral 200 denotes a lead frame, 201 inner terminal portions, 202 outer terminal portions, 203 connecting lead portions, 204 a connecting portion, and 205 an outer frame portion, respectively. The lead frame is made of 42 ALLOY (namely, an Fe alloy containing 42% Ni). The lead frame has a thickness of 0.05 mm at its thinner portion, that is, the inner terminal portions, and a thickness of 0.2 mm at its thicker portion, that is, the outer terminal portions. The connecting portion, which connects facing tips of the inner terminal portions to each other, has a thickness of 0.05 mm corresponding to that of the thinner portion. This connecting portion has a structure capable of allowing an easy punching thereof in the fabrication of the semiconductor device, as described

hereinafter. Although the outer terminal portions 202 have a ball shape in the illustrated embodiment, they are not limited to this shape. Also, although the lead frame has been described as being made of the 42 ALLOY, it is not limited to this material. For the lead frame, a copper-based alloy may be used.

Now, fabrication of the lead frame according to the illustrated embodiment will be described in brief. Fig. 4 illustrates a process for fabricating the lead frame according to the illustrated embodiment. First, a lead frame blank 300 having a thickness of 0.2 mm was prepared which is made of a 42 ALLOY (an Fe alloy containing 42% Ni). The prepared lead frame blank 300 was then subjected to a cleaning process, thereby removing grease from the surfaces thereof (Fig. 3a). Subsequently, photoresist films 301 were coated over both surfaces of the lead frame blank 300, respectively. The coated photoresist films 301 were then dried (Fig. 3b).

Using desired pattern plates, the photoresist films 301 on both surfaces of the lead frame blank 300 were exposed to light at their desired portions. A developing process was then conducted to the light-exposed photoresist films 301, thereby forming photoresist patterns 301A.

For the photoreist films, a negative liquid-phase resist (PMER resist) manufactured by Tokyo Ohka Co., Ltd.

was used. Using the resist patterns 301A as anti-etch films, the lead frame blank 300 was subjected to a spray etching process at both surfaces thereof. The spray etching process was conducted using a ferric chloride solution of 48 BAUME at 57 °C. Thus, a lead frame having a structure of Fig. 2a was obtained (Fig. 3d). Fig. 2a is a plan view of the lead frame. Fig. 2b is a cross-sectional view taken along the line A1 - A2 of Fig. 2a. Thereafter, the remaining photoresist thin films were peeled off. The resulting structure was then subjected to a cleaning process. A gold plating process was subsequently conducted for desired portions of the lead frame, that is, regions including inner terminal portions (Fig. 3e).

In the fabrication process of the lead frame, the etching process was conducted with a large etch depth at one major surface of the lead frame blank where outer terminal portions are to be formed, and with a small etch depth at the other major surface of the lead frame. In place of the gold plating, silver or palladium plating may be utilized. The above mentioned lead frame fabrication process is adapted to manufacture a single lead frame required for the manufacture of a single semiconductor device. In terms of productivity, however, the etching process is conducted for lead frame units each corresponding to the single lead frame shown in Fig. 2. To

this end, a frame member (not shown) is provided at a desired portion of the peripheral edge of the lead frame so as to connect a desired part of the outer frame portion 205 shown in Fig. 2 to a corresponding one of an adjacent lead frame.

Using the lead frame fabricated as mentioned above, the resin encapsulated semiconductor device according to the present invention was fabricated. Now, a method for fabricating the resin encapsulated semiconductor device in accordance with an embodiment of the present invention will be described. Fig. 4 illustrates the method for fabricating the resin encapsulated semiconductor device in accordance with the embodiment of the present invention. A polyimide-based thermosetting insulating adhesive (tape) 401 (HM122C manufactured by Hitachi Chemical Co., Ltd.) was applied to one surface, formed with the outer terminal portions 402, of the lead frame 400 fabricated as in Fig. 3 and the outer surface of the lead frame 400 using a hot pressing process conducted at 400 °C and 6 Kg/m^2 for 1.0 second Fig. 4a). The resulting structure is shown in Fig. 5 which is a plan view. Thereafter, the connecting portions 403 connecting facing tips of the inner terminal portions were punched using punching dies 405A and 405B (Fig. 4b). Also, portions of the insulating adhesive

(tape) corresponding to those connecting portions 403 were punched (Fig. 4c)

Subsequently, unnecessary portions of the lead frame including the outer frame 404 were cut off using outer frame punching and pressing dies 406A and 406B (Fig. 4d). The lead frame was then bonded to a semiconductor chip 407 at its leads 410 under pressure while applying heat (Fig. 4e).

The process for cutting off the unnecessary portion of the lead frame including the outer frame 404 supporting the the entire portion of the lead frame along with the connecting lead portion, as shown in Fig. 4d, may be carried out after an resin encapsulating process. In this case, dam bars (not shown) are preferably provided, as in QFP packages typically using a lead frame having a single layer structure. After the mounting of the leads 410 on the semiconductor chip 411, the inner terminal portion 410 of each lead 410 was electrically connected to an associated one of terminals (pads) 411A of the semiconductor chip 411 (Fig. 4f).

Subsequently, an epoxy-based resin 415 was molded to encapsulate the resulting structure while exposing the outer terminal portions 410B of the leads 410 using a desired mold (Fig. 4g).

Although a specific mold (not shown) was used for the above process in the illustrated case, use of such a die may be unnecessary in so far as the resin encapsulating process can be conducted under the condition in which desired portions (outer terminal portions) of the lead frame are left. Thereafter, a solder paste was coated on the exposed outer terminal portions 410B in accordance with a screen printing process, thereby forming outer electrodes 416 made of solder (paste). Thus, the fabrication of the resin encapsulated semiconductor device according to the present invention was achieved (Fig. 4h).

Although the formation of the outer electrodes 416 made of solder has been described as being achieved using a screen printing process, it may be achieved using a reflow or bonding process in so far as an amount of solder required for a connection of the semiconductor device to a circuit board is obtained.

[EFFECTS OF THE INVENTION]

As apparent from the above description, the present invention makes it possible to increase the occupancy degree of a semiconductor chip in a semiconductor package in situations requiring new resin encapsulated semiconductor devices having a highly integrated structure while exhibiting a high performance. The present invention

also makes it possible to reduce the area of the semiconductor device on a circuit board in order to cope with a compactness of the semiconductor device. That is, the present invention can provide a semiconductor device capable of achieving an improvement in the mounting density on a circuit board. At the same time, the present invention can provide a resin encapsulated semiconductor device having a new multipinned structure which could not be realized in compact packages such as conventional TSOPs.